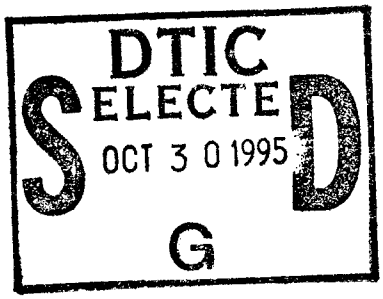
RL-TR-95-187
In-House Report
September 1995

A REVIEW OF SELECTED SMART PIXELS: SELF ELECTRO-OPTIC EFFECT DEVICES, SURFACE EMITTING LASER LOGIC DEVICES, DOUBLE HETEROSTRUCTURE OPTO-ELECTRONIC SWITCH, DIODE LASER LOGIC, QUENCHED-LASER OPTICAL GATES

M.A. Parker, R.J. Michalak, J.S. Kimmet, W.A. Davis,
S.I. Libby (Rome Laboratory), D.B. Shire,
C.L. Tang (Cornel University)



APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

Rome Laboratory
Air Force Materiel Command
Griffiss Air Force Base, New York

This report has been reviewed by the Rome Laboratory Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RL-TR-95-187 has been reviewed and is approved for publication.

APPROVED: James W Cusack

JAMES W. CUSACK, Chief
Photonics Division
Surveillance & Photonics Directorate

FOR THE COMMANDER: Donald W. Hanson

DONALD W. HANSON
Director of Surveillance & Photonics

If your address has changed or if you wish to be removed from the Rome Laboratory mailing list, or if the addressee is no longer employed by your organization, please notify RL (OCPA) Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	September 1995	In-House

4. TITLE AND SUBTITLE A REVIEW OF SELECTED SMART PIXELS: SELF ELECTRO-OPTIC EFFECT DEVICES, SURFACE EMITTING LASER LOGIC DEVICES, DOUBLE HETEROSTRUCTURE OPTO-ELECTRONIC SWITCH, DIODE LASER LOGIC, QUENCHED-LASER OPTICAL GATES

5. FUNDING NUMBERS
PE - 62702F
PR - 4600
TA - P3
WU - 22

6. AUTHOR(S) M.A. Parker, R.J. Michalak, J.S. Kimmet,
W.A. Davis, S.I. Libby (Rome Laboratory)
D.B. Shire, C.L. Tang (Cornell University)

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Rome Laboratory (OCPA)
25 Electronic Pky
Griffiss AFB NY 13441-4515

Cornell University
School of Electrical
Engineering
Ithaca NY 14853

8. PERFORMING ORGANIZATION REPORT NUMBER
RL-TR-95-187

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (OCPA)
25 Electronic Pky
Griffiss AFB NY 13441-4515

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Michael A. Parker/OCPA/(315)330-7671

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This report contains technical details on several popular types of smart pixels including Self Electro-optic Effect Devices (SEEDs), Surface Emitting Laser Logic Devices (CELLs), Double Heterostructure Opto-electronic Switches (DOES), Diode Laser Logic (DLL), Laser-Quenched Laser (LQL) Optical Gates. Of these devices, the SEED is the most developed and considerable detail is included on the R, D, S, and F SEEDs. The CELL devices consist of Heterostructure Bipolar Transistors (HPTs) integrated with Vertical Cavity Surface Emitting Lasers (VCSELs). The DOES consists of integrated Optical thyristors and In-Plane Lasers (IPLs). DLL devices form a complete logic fanily and they are composed of integrated Q-switched IPLs, detectors and current sources. The LQL optical gates offer the highest speed performance of the smart pixels. They consist of cross coupled lasers. The CELLs, DOES, DLL and LQL devices are still in the research phase at the time of this report. As a result, preliminary data is presented on their performance characteristics.

14. SUBJECT TERMS
optoelectronics, SEEDs, lasers, smart pixels

15. NUMBER OF PAGES
68

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	U/L

ACKNOWLEDGMENTS

The authors wish to acknowledge members of the Photonics Center, the National Nanofabrication Facility and Cornell University for helpful discussion during the course of the smart pixel work. The authors acknowledge J. Cusack and B. Hendrickson for encouragement and financial support, and J. L. Rossi for assistance with the government contracts, and R. Boncek and C. J. Parker for valuable comments and corrections on the contents of this report. In addition, the authors thank VIXEL Inc., Intelligent Automation and AT&T for permission to reproduce some of their figures. Please refer to the references for the citation.

All authors contributed to the work presented in this report. M. A. Parker researched and wrote the report and designed several of the reported devices. M. A. Parker, J. S. Kimmet, and R. J. Michalak fabricated and tested the Diode Laser Logic and Laser Quenched Logic gates. W. A. Davis, D. B. Shire and C. L. Tang along with the other authors worked with new versions of the LQL gates and provided valuable technical insight. S. I. Libby managed the phase I and phase II SBIRs for Photonics Research Inc. and experimentally invesitaged the feasibility of their early CELL devices.

TABLE OF CONTENTS

I. INTRODUCTION

Signal processors are presently limited by the performance of the electronic logic gates and the electrical interconnections between those gates. Compared with projections for the performance of optical devices, present logic elements are slow in addition to their large power requirements.

There are two significant problems with present semiconductor device architectures that concern the interconnect. The first concerns the two dimensional aspect of integrated circuits where data signals are confined to a plane. Here, the complexity and density of the interconnections increases faster than that for the devices.[1] Integrated circuit manufacturers now use multiple levels of metal interconnections between planar logic devices to overcome this problem, but this approach still has limitations, too. The second problem concerns the electrical nature of the interconnects. The bandwidth is limited by resistive and capacitive effects. In addition, the cross talk between channels and the power required to drive the interconnect increases with the driving frequency.

These problems can be solved by the use of interconnects that are optical rather than electrical ones. The preferred architecture for signal processors and communication systems makes use of a set of stacked wafers that communicate with each other by light. The use of out-of-plane optical interconnects increases the parallelism of the data link and, hence, also the speed of the system through efficient use of these dimensions.

The devices that produce or modulate the light in these interconnects can also be given logic functions. Thus, in effect, one device (smart pixel) can serve as a logic

element and as an interconnect. Smart pixels are generally viewed as single devices or small clusters of devices. Smart pixels can also be divided into at least two different types. The first type is the all-optical smart pixel. In this case, one or several beams of light interact within a small volume of matter to produce a resultant beam. The light must interact with the electric charge in the material to produce the desired effect. The other type is the opto-electronic hybrid that has both optical and electronic components. In this case, photodetectors intercept the input light signals, electronic components implement a logic function and an optical transmitter generates the resultant beam. With clever enough designs, there would be little distinction between the all-optical and opto-electronic hybrid devices since both involve the interaction between light and electronic charge.

There are many different types of smart pixels. Monolithically integrated field effect transistors (FETs) and lasers have been available since the 1980's but they are only recently appearing in smart pixel designs. The AT&T self electro-optic effect devices (SEEDs) are probably the most developed of the smart pixels. However, most other types of smart pixels are still research grade devices. Because of the relative newness of these devices, several different types of smart pixels will be considered including the various types of SEEDs, the surface-emitting laser logic devices (CELLs), double-heterostructure opto-electronic switch devices (DOES), and laser quenched logic devices (LQLs).

II. SEEDs

SEEDs were developed as opto-electronic hybrids to bring optics into the realm of processing.[2] Large two dimensional arrays of SEEDs can be used as transmissive or

reflective electro-optic modulators. The difference concerns only the manner in which the SEED handles the input and output light signals. In the transmissive mode, light enters one end of the SEED from a direction perpendicular to the 2D array and exits at the opposite end as a modulated light signal. In the reflective mode, light also enters the SEED perpendicular to the array. However, it is then modulated and reflected back out parallel to the incident beam but in the opposite direction. The reflective SEED is most commonly used since it is less sensitive to heat, has lower insertion loss and has greater modulation depth. Generally, these arrays are optically interconnected through free space using bulk optics.[3]

The SEED in its most basic form is derived from an electro-optic absorption modulator (EOAM). An EOAM consists of a semiconductor PIN diode structure with multiple quantum wells in the intrinsic I region as shown in Figure 1[4]. Light enters the EOAM through the N-doped semiconductor and passes through the GaAs quantum wells and the $Al_{0.35}Ga_{0.65}As$ barriers. The light reflects off the Bragg reflector mirror stack which consists of alternating quarter-wave layers of GaAs and $Al_{0.19}Ga_{0.81}As$. The light then passes through the quantum wells for a second time where it is further modulated. The N and P semiconductors are used to apply bias voltage to the quantum wells so as to modify their absorption characteristics using the quantum confined stark effect (QCSE).

The structure of Figure 1 is taken to form the basic SEED element and can operate as either a type of reverse-bias voltage-controlled photodetector or modulator. A PIN diode

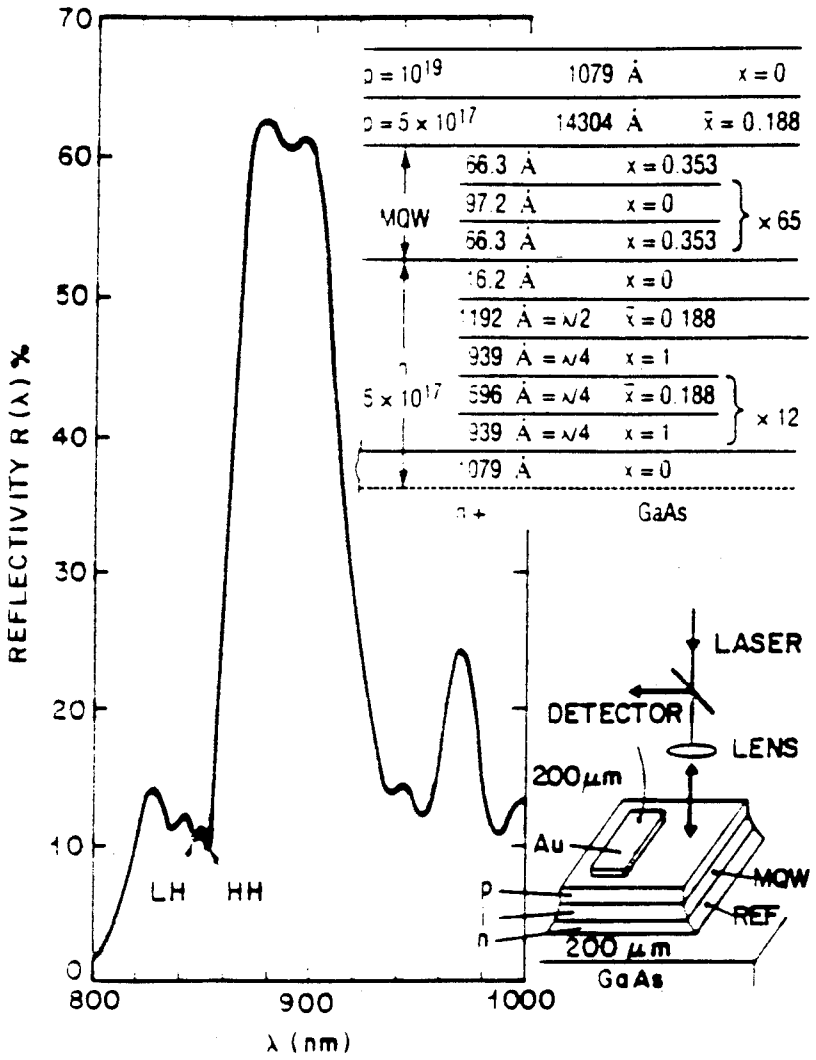


Figure 1: Structure of the MQW reflection modulator and a typical reflectivity spectrum of the wafer (with antireflection coating). x is the fraction of AL in the $Al_xGa_{1-x}As$.

photodetector produces a photocurrent J that is related to the incident optical power P_{opt} according to

$$J = RP_{opt} \tag{1}$$

where R is the responsivity. Normally, photodetectors that operate at wavelengths shorter than (*i.e.*, energies above) the energy bandgap of the semiconductor material have a responsivity that is essentially independent of the magnitude of the applied reverse bias. However, the situation is different for a QCSE photodetector operated near the energy bandgap wavelength. In this case, the optical absorption of the quantum wells greatly depends on the applied reverse-bias voltage. Thus the photocurrent and hence, the responsivity, are also bias voltage dependent. As a note, the SEED can perform as a normal PIN diode photodetector for wavelengths sufficiently far from the exciton absorption energies.

The SEED, as an EOAM, relies on the ability of the applied bias voltage to alter the effective reflectivity R_{eff} of the SEED. Here, R_{eff} is defined as the ratio of the output optical intensity to the input optical intensity. Changes of the reverse bias voltage alter the optical absorption of the quantum wells and, thus, also the intensity of the light passing through the SEED.

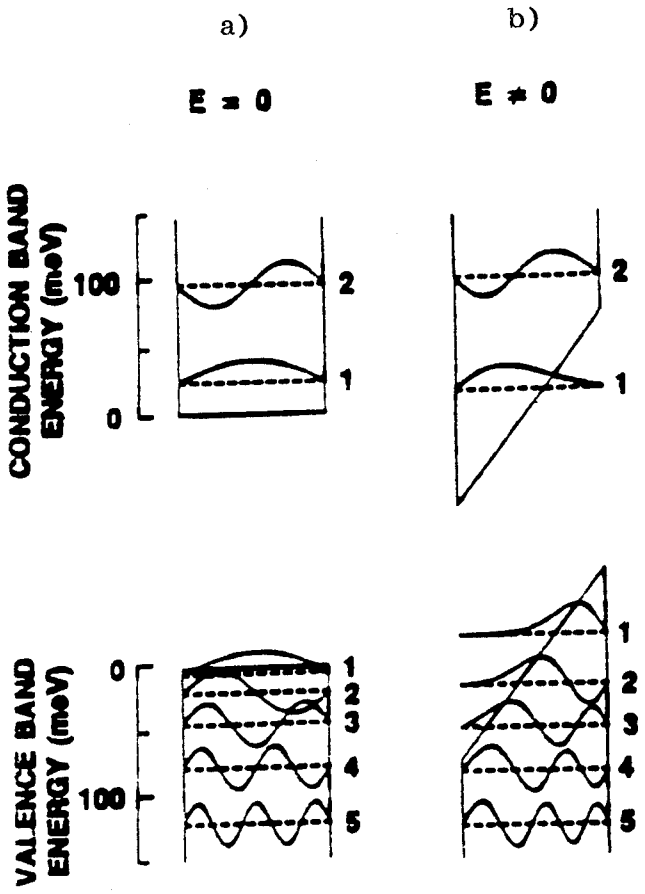


Figure 2: Energy band structure of a quantum well a) without an applied electric field and b) with an applied electric field.

The QSCE [5] is responsible for the effect that an electric field has upon the optical absorption in the PIN diode structure of Figure 1. Figure 2a shows the band gap diagram for the quantum wells without an electric field present. The GaAs forms a quantum well for both the conduction and valence bands because its bandgap is smaller than that of the surrounding AlGaAs. For simplicity, the distinction between light and heavy holes is neglected. The figure shows the energy levels for both electrons and holes. The narrow wells force the hole and electron wavefunctions to overlap and the Coulomb interaction causes the formation of an exciton or spatially confined electron-hole pair. In some respects, the exciton can be described by a hydrogen-like model. In bulk semiconductors without the wells, the carrier pairs still form excitons but they have short lifetimes since they are easily ionized. The increased overlap of the wavefunctions in the quantum wells results in an increased lifetime and an increased binding energy for the exciton. Figure 9.2b shows an energy band diagram for finitely deep quantum wells in the presence of an electric field. The triangular shape of the potential well decreases the energy difference between the electron and hole states and pushes the two particles to opposite sides of the well.[6] Thus the energy required to produce an exciton is reduced and, as a result, the absorption curve shifts to longer wavelenths. The decreased overlap between the two wavefunctions results in a decrease in the peak of the absorption. Figure 3 shows three typical absorption curves for the SEEDs for three different bias voltages.[7] Each curve is shown with two maxima. The largest maxima corresponds to the formation of excitons with electrons and holes in their corresponding lowest energy levels (n=1), the heavy hole

exiton transition. The smaller maxima corresponds similarly to the n=2 light hole exciton transition.

The operation and application of the SEEDs are derived from the absorption curves in Figure 3. Normally, an application is designed for either λ_0 or λ_1 operation. For the case of λ_0 operation, the wavelength of the light is set at the peak of the n=1 exciton in the absence of any external bias applied to the SEED. An applied reverse bias voltage causes the peak to shift to longer wavelengths and the absorption at the operating wavelength tends to decrease. Note that the curve biased at 10 V has the n=2 exciton peak at the operating wavelength and, as a result, the absorption has actually increased slightly compared with the 5V bias curve. For the preferred λ_1 mode, the operating wavelength is set to a wavelength larger than the n=1 exciton peak. In this case, increases in reverse bias voltage tend to increase the optical absorption. The reflectivity and responsivity of the SEED are shown in Figure 4 for λ_1 operation. For the proper range of reverse bias voltage, the photocurrent from the PIN structure increases since the responsivity increases and the intensity of the reflected light decreases.

SEEDs are fabricated into a variety of circuits. The R-SEED and D-SEED consist of the series combination of a SEED with a resistor and a diode, respectively. These are the simplest combinations to exhibit bistablility. The Symmetric SEED or S-SEED consists of two SEEDs in series. They are intended for dual rail or differential optical input applications. The F-SEED is a SEED monolithically integrated with a field effect transistor.

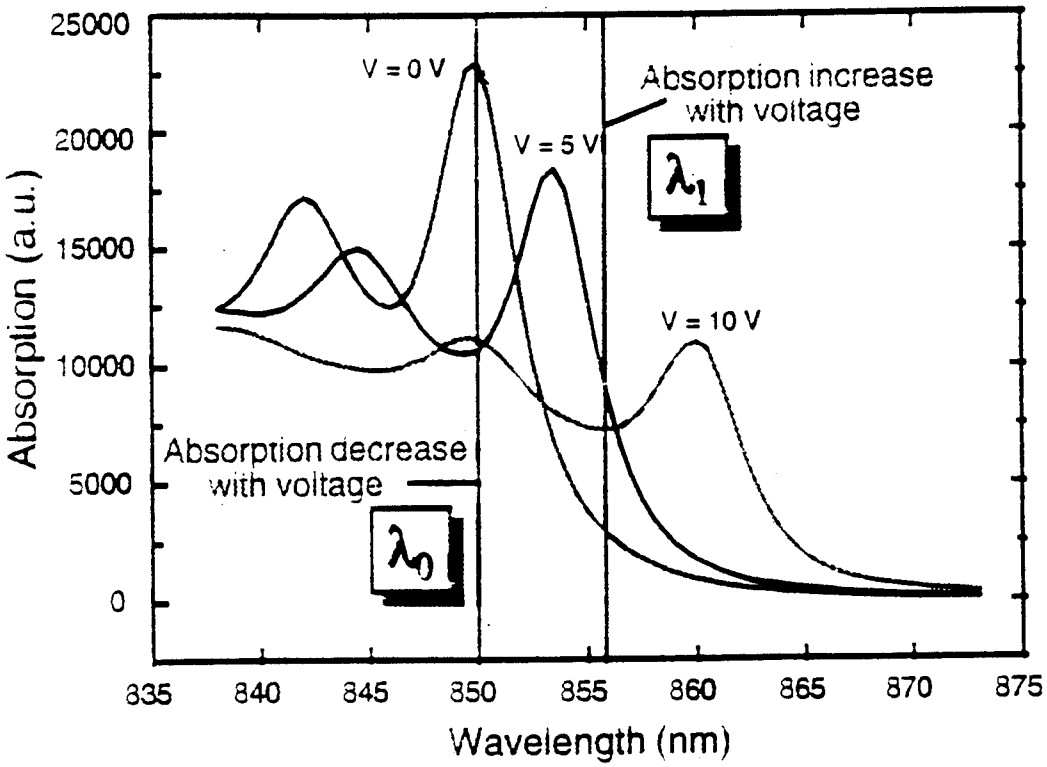


Figure 3: Absorption spectra of an EOAM for bias voltages of 0, 5 and 10 V.

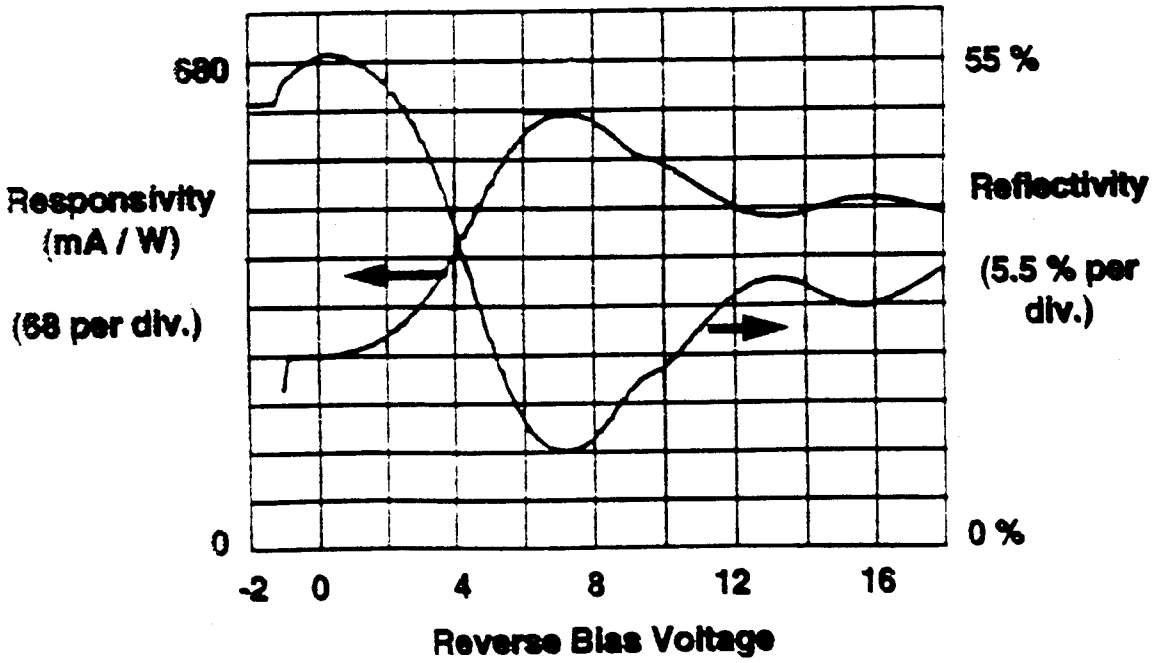
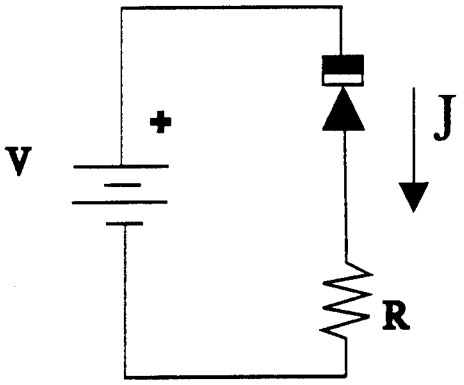


Figure 4: Reflectivity and responsivity for 500 μW incident power at 850 nm wavelength in a 3 μm diameter spot current FET-SEED modulator design operated at λ_1 (wavelength longer than zero-field exciton peak).

a)



b)

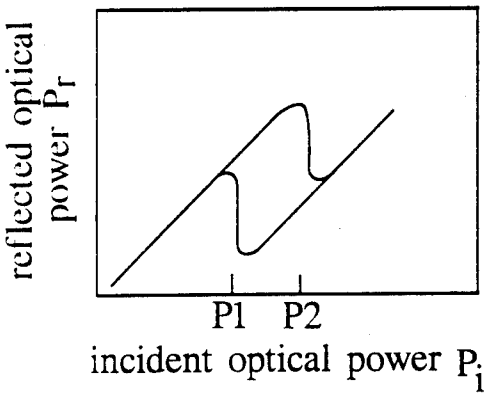


Figure 5: a) R-SEED configuration. b) R-SEED transfer function.

IIA. R-SEED

The R-SEED consists of a SEED integrated in series with a resistor as shown in Figure 5. The device is operated at λ_0 so that the absorption of the SEED increases with decreasing voltage; this configuration sets up a positive feedback situation.[7] Light of wavelength λ_0 incident on the SEED is absorbed and produces photocurrent J in the direction shown. Consider the upper branch first. Initially, as the incident power P_i increases, the reflected power P_r also increases as is appropriate for relatively constant reflectivity and absorption. However, the generated photocurrent J from absorbed photons increases the voltage drop across the resistor and thus reduces the voltage across the SEED. As the incident power further increases, the voltage across the seed reduces further and the peak in the absorption curve moves closer to λ_0. All along the upper branch, the absorption is relatively low. Only at incident power P_2 does the absorption curve center at λ_0. At this point, the absorption increases greatly and the effective reflectivity drops. Further increases in incident power appear as a reflected signal described by branch 2. The difference between branch 1 and 2 is that the SEED is in a highly absorbing state along branch 2 and thus, the SEED is producing significantly more photocurrent even at power P_2 than it did along branch 1. Thus, along branch 2, the incident power can be lowered to P_1 before the voltage across the SEED shifts the absorption curve away from λ_0. At this point, the system shifts back up to the top branch. The width of the hysteresis loop is controlled by several factors including the voltage

required to move the absorption peak to λ_0, the value of the series resistance, and the difference between the absorption maximum and minimum.

The D-SEED is similar to the R-SEED except that a conventional photodiode replaces the resistor. The conventional photodiode is basically an optically controlled current source where the photocurrent is essentially independent of the reverse bias voltage. In this case, the load for the SEED can be set by an external optical signal incident on the photodiode. Such a combiniation yields better switching characteristics.[7]

The Self-Linearized Modulator (S-LM) [8], shown in Figure 6, is also related to the R-SEED. The current source replaces the series combination of the voltage source and resistor. Unlike the R-SEED, however, the S-LM is operated at λ_1 where the absorption increases with reverse bias voltage. Assume that the S-LM is operated in a range of bias voltage such that the quantum efficiency is unity (i.e. one electron-hole pair of carriers is created for every absorbed photon). The current J, set by the current source, must be identical to the photocurrent produced in the SEED since only negligibly small conduction currents flow through a reverse biased PIN structure. The voltage across the SEED adjusts the absorption in such a way that the number of absorbed photons produces the correct number of carriers for the photocurrent J. Thus,

$$P_i - P_o = \frac{hc}{e\lambda_1} J \tag{2}$$

where h is Plank's constant, c and λ_1 are the speed and wavelength of the light in vacuum, respectively, and e is the elementary charge.

IIB. S-SEED

Some applications require a number of simple SEED circuits to be interconnected or cascaded. Such arrangements require optical gain (fan-out larger than 1) and good on-off contrast ratio. However, a single SEED absorbs power from the optical signal and the contrast ratio can be as low as 2:1. The symmetric or S-SEED alleviates these problems and offers significant advantages for the optical system.

The S-SEED consists of two SEEDs electrically connected in series and uses two parallel optical signals at λ_0 for input and output. One SEED serves as the load for the other as shown on the left side of Figure 7a. Two incident optical signals (P_1 and P_2) with equal intensity produce identical photocurrents in the two SEEDs so that the voltage V_1 at the node between them does not change. Only a change from unity in the ratio P_1/P_2 can toggle the S-SEED between stable states. An S-SEED can be used as the output modulator for a logic circuit as shown in Figure 7b. Two FETs force the voltage at the common node to change and thereby switch the S-SEED between states. This dual-rail input and output using two parallel optical signals has several advantages over the single ended input and output. First it allows for time-sequential gain where relatively weak optical signals set the state of the S-SEED and two strong optical signals of equal intensity read the state of the device. The read-out beams have equal intensity to ensure that the S-SEED remains in the original state. The fact that the read out beams have larger intensity

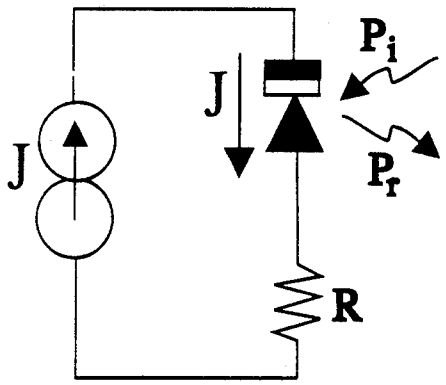
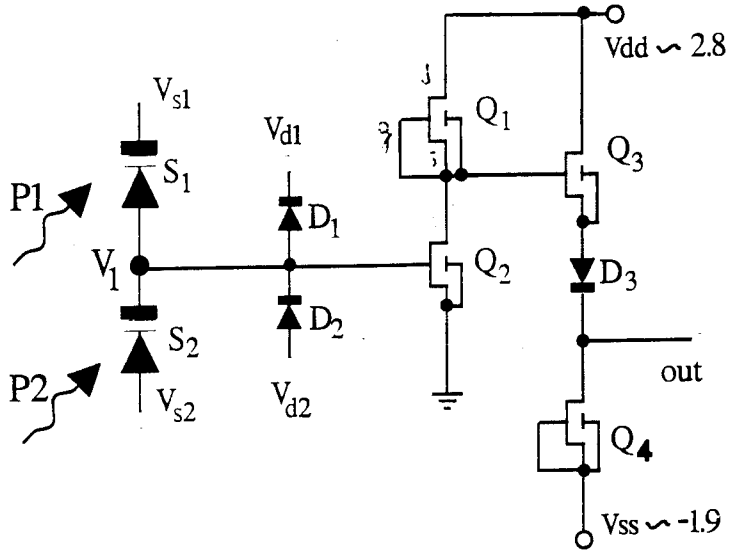


Figure 6: Self-Linearized Modulator.

a)



b)

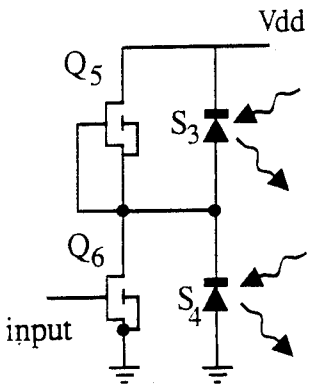


Figure 7: a) F-SEED receiver, where S-SEED forms the front end. b) F-SEED transmitter.

than the set beams means that more optical power is available for succeeding stages. The contrast ratio of the SEED no longer matters very much since a factor of two (or more) change in P_1/P_2 from unity is sufficient to switch states. Furthermore, the dual-rail architecture provides a convenient method for representing +1, 0, and -1 as, for example, by $P_1/P_2 > 1$, $P_1/P_2 = 1$ and $P_1/P_2 < 1$, respectively.

IIC. F-SEEDs

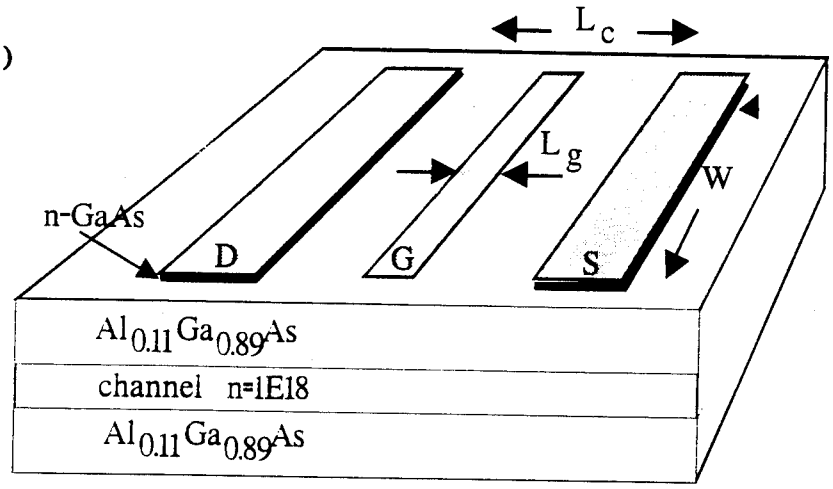
The F-SEED consists of an S-SEED monolithically integrated with a field effect transistor (FET). The F-SEED has optical input and output, and electronics to process logic functions. Figures 8a and 8b shows the structure of the F-SEED. The F-SEEDs do not need optical bistability[9] and can be operated at longer wavelengths than the exciton peak. The doped-channel MISFET-like Transistor (DMT)[9,10] is epitaxially grown on top of the SEED structure that has the P-side on the bottom. The 900 angstrom thick spacer layer functions as the insulator for the gate and the 200 angstrom buffer serves as an insulator between the FET and SEED structures. Source and drain electrical contacts are evaporated on top of the 1000 angstrom n-layer with further processing to make Ohmic contact with the n-channel. The SEED is epitaxially grown on top of a semi-insulating substrate. This type of substrate allows adjacent devices to be electrically isolated from each other. The P-type electrical contacts are made from the top side. As shown by the circuit symbols for the FETs in Figure 7, the source is electrically connected to a "backplane." This backplane is the p+ conducting layer below the SEED MQW region.

The p+ layer prevents stray electrical fields from affecting the carrier concentration in the channel of neighboring FETs. Thus the p+ layer shields each FET. Light can easily propagate through the n-channel DMTs as is required for the operation of the SEEDs[9,11].

Figures 8a and 8b show typical F-SEED circuits.[12] SEEDs S1 and S2 couple optical signals to the FETs. Voltage V_1 varies between V_{s1} and V_{s2} under the control of the optical signals. The voltage on the gate of FET Q2 relative to the voltage on the source should swing from -1 to +1 V. Gate voltages lower than -1 V have negligible effect on the drain current and might cause the transistor to break down. Gate voltages larger than approximately +1 V cause charge to be transferred between the gate and the channel.

Thus, large voltage swings in V_1 must be limited. Diodes D1 and D2 clamp the gate voltage to the range $V_{d2}-0.9<V_1<V_{d1}+0.9$. The F-SEED circuits consist of buffered FET logic (BFL) Devices. Figure 7a is a BFL inverter that consists of transistors Q1 through Q4 and diode D3. Transistor Q1, which has a gate to source voltage of zero, serves as the load for Q1. The voltage on the source of transistor Q3 follows the voltage on the gate and they are essentially equal. Transistor Q4 is the load and diode D3 level shifts the voltage for the next gate. The level shifting diodes are necessary since the input stage of a logic gate (Q1 and Q2) always has a source tied to ground. The output voltage V_2 swings from -0.4 to 0.9 V. A second diode in series with D3 is sometimes used to further shift the voltage for different operating voltages. In addition, Q3 can be omitted

a)



b)

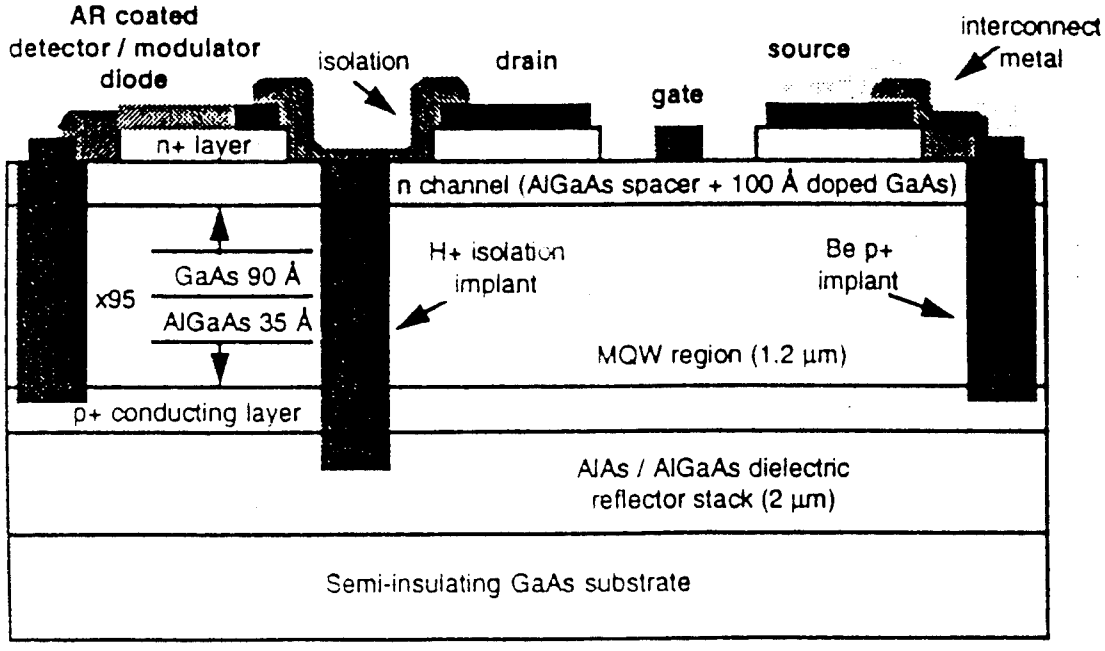
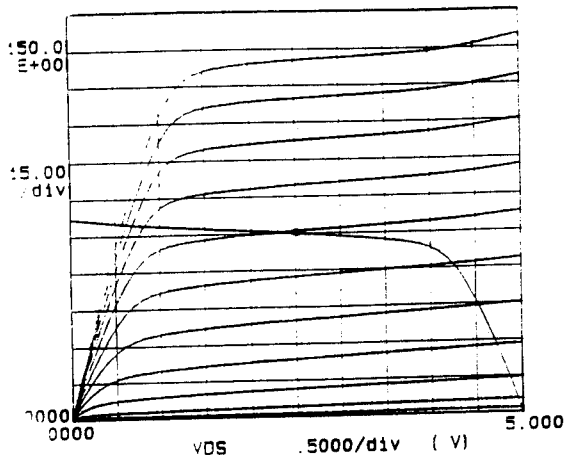
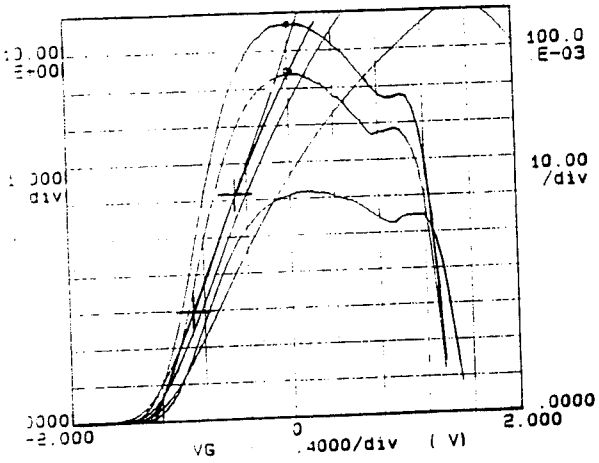


Figure 8: a) DMT for the F-SEED. b) F-SEED cross-section.

a)



b)



c)

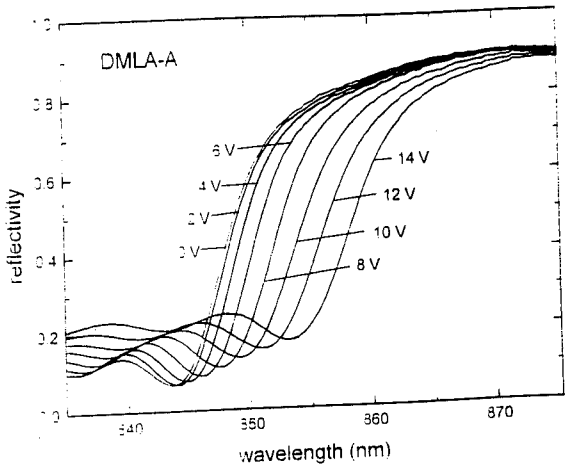


Figure 9 a) Plots of J_D *vs* V_{DS} at values of V_{GS} from -1.2V to +0.8V at 0.2V intervals for a 20 μm wide FET. Superimposed is a load FET curve where V_{GS}=0V, (also 20μm wide). b) FET transfer function. c) SEED reflectivity spectra *vs* applied bias.

under certain conditions and the logic gate becomes unbuffered. A modulator circuit appears in Figure 7b. The voltage at the juction of transistors Q5 and Q6 modulates the voltage across the two SEED devices and, thus, also the reflectivity of the SEEDs.

Typical FET dimensions also appear in Figure 8a. The gate width L_g is 1 μm and the channel length L_c is 5 μm. The characteristic curves for this device appear in Figure 9a. The vertical axis represents the ratio of drain current I_d to the gate width W. The figure shows that FETs with W = 10 μm typically have drain currents of 1 mA. The FETs can have channel widths W as large as 70 μm. Figure 9b shows the typical transfer function. Typical reflectivity as a function of bias voltage and wavelength for the SEEDs appear in Figure 9c.

The SEEDs and FETs can be combined into many novel and useful configurations. Some of the optical processing applications include edge detection, spatial differentiation, Laplacian operators and neural nets. These systems are made of more elemental circuits such as other logic gates, transimpedance amplifiers, and differential amplifiers.

III. Surface Emitting Laser Logic Devices

As is evident, SEEDs support a 3-dimensional architecture where the optical signals enter and leave perpendicular to the plane containing the SEED circuits. Such an architecture is important for signal processing applications where a large number of optical interconnections are required to handle large amounts of parallel data flow. Other smart pixel designs use integrated lasers to produce the optical signals. The vertical cavity surface emitting laser (VCSEL) is an ideal emitter for the 3-dimensional architecture.

Photonics Research Inc. (PRI -- now VIXEL Corp.)[13] is developing surfaCe-Emitting Laser Logic (CELLs) devices for multi-layer signal processing. Figure 10a shows the epi-material and device layout. The CELLs consist of a VCSEL and a heterostructure photo-transistor (HPT) that are electrically connected in series. As shown in Figure 10b, the VCSEL has distributed bragg reflector (DBR) mirror stacks that consist of quarter-wave thick alternating layers of GaAlAs and AlAs. The multiple quantum well (MQW) active region is positioned between the mirror stacks. The HPT npn layers are grown on top of those for the VCSEL. Normally, the top mirror stack is almost 100% reflective and so little light enters the HPT from the VCSEL. Thus the epitaxial growth naturally defines a series electrical connection between the HPT and the VCSEL.

Typical performance data from early devices appear in Figures 11 and 12. The VCSEL has a threshold current on the order of 10 mA. Figure 11 shows typical characteristic curves for the HPTs. Figure 12 shows the output optical power from the VCSEL versus the input optical power to the HPT and Figure 12 shows the circuit schematic. Below 70 mW of input power, the HPT does not supply enough current to the VCSEL for it to lase. For sufficiently intensity input optical power, the VCSEL lases and the CELL has optical gain exceeding a factor of 20. The graph also indicates an on/off contrast ratio larger than 40 to 1. The inset to Figure 12 shows the single mode lasing spectrum from the VCSEL.

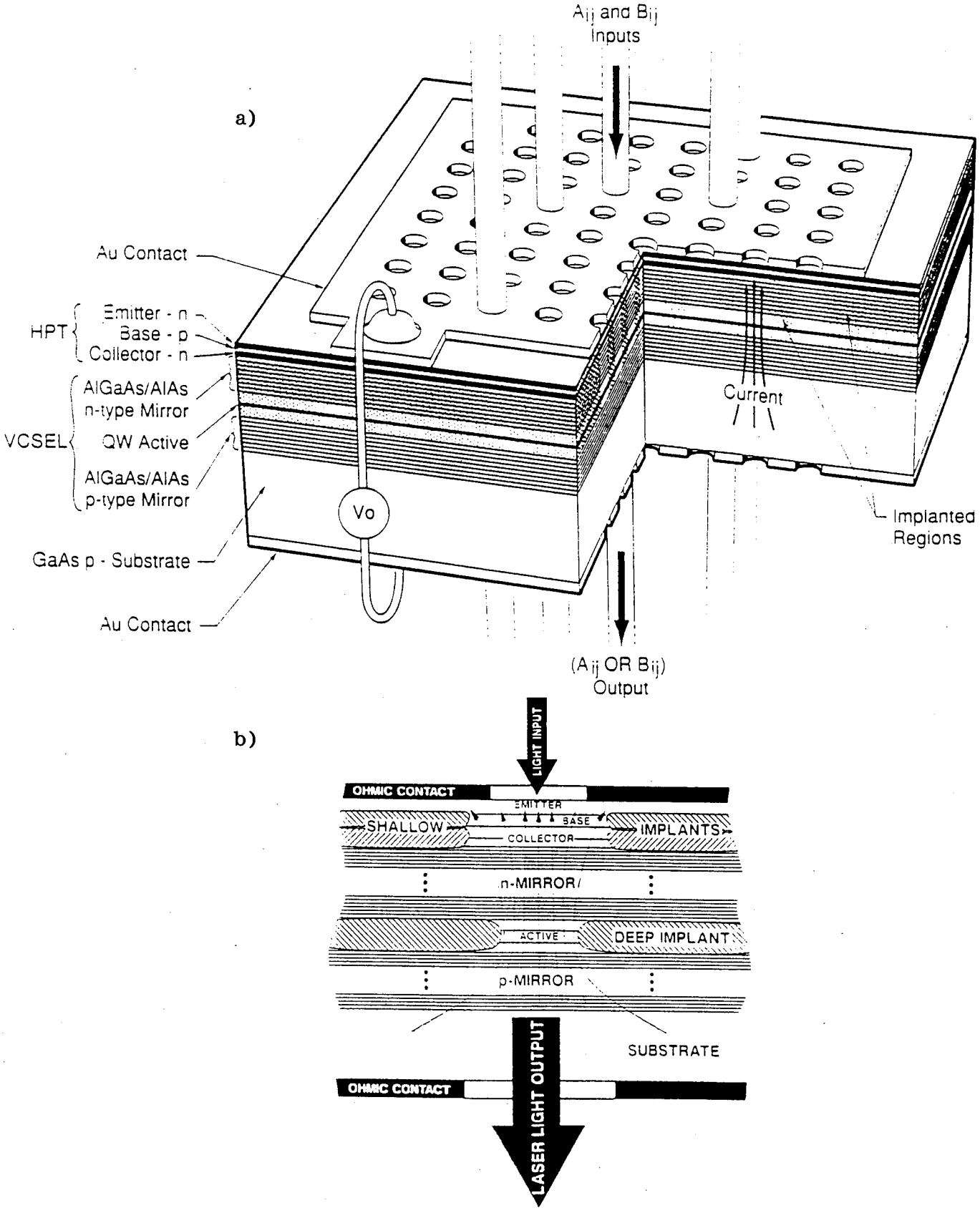


Figure 10: a) CELL device layout and material cross-section. b) VCSEL cross-section.

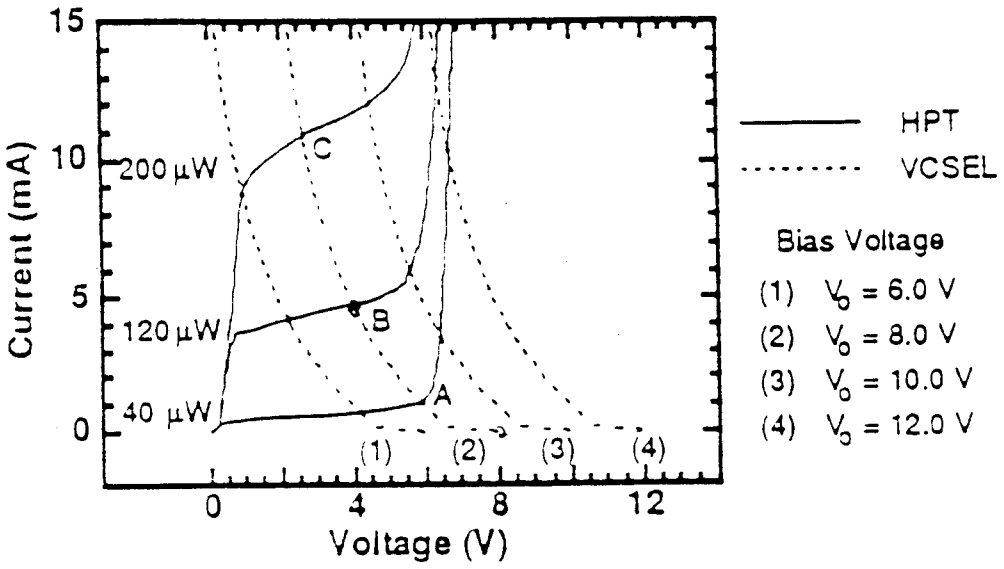


Figure 11: HPT and VCSEL current/voltage characteristics.

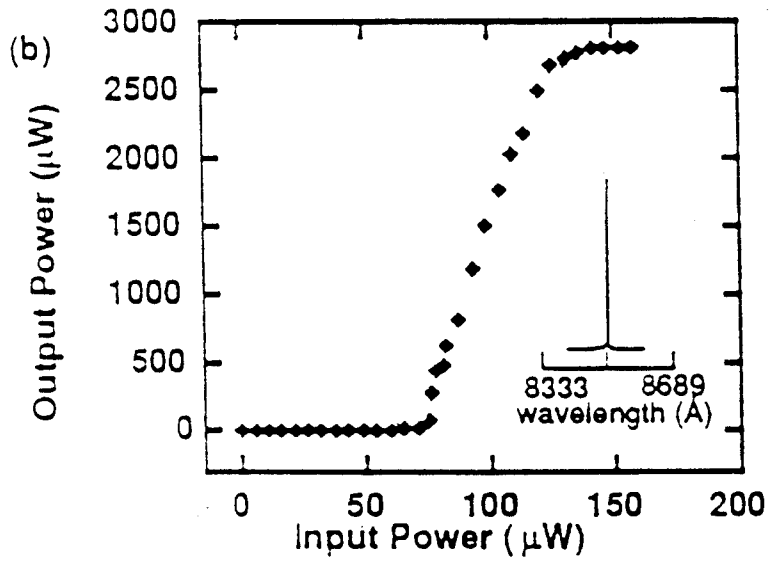


Figure 12: VCSEL output/HPT input transfer function.

The CELL device can be connected in a variety of configurations to perform various logic functions. Figure 14 shows the AND, OR and XOR configurations and the oscilloscope graphs. The AND configuration requires the combined intensity of two beams for the HPT to provide sufficient current to the VCSEL for it to lase. For the OR configuration, either of two input beams have enough power to produce the result. The XOR operates as follows. One or the other of the two VCSELS will lase when the voltage at the emitter-collector node is above +V or below -V. The voltage at the node V_{node} is controlled by the ratio of the two input beams A and B. If A > B then V_{node} = +V and if B > A then V_{node} < -V. However, similarly to the SEED, if the ratio A/B remains constant then there is no change in the output state of the device.

The CELL device can also be used as an optical amplifier or an optical memory element. The CELL can be operated as an optical amplifier in the linear portion of of the curve of Figure 12. An optical memory element would function as follows. As previously mentioned, the top mirrorof the VCSEL is nearly 100% reflective. If this value is reduced slightly, an optical signal from the VCSEL will produce positive feedback from the HPT. With sufficient feedback, the VCSEL will latch in the "ON" state. Additional circuity must then be included to reset the memory element.

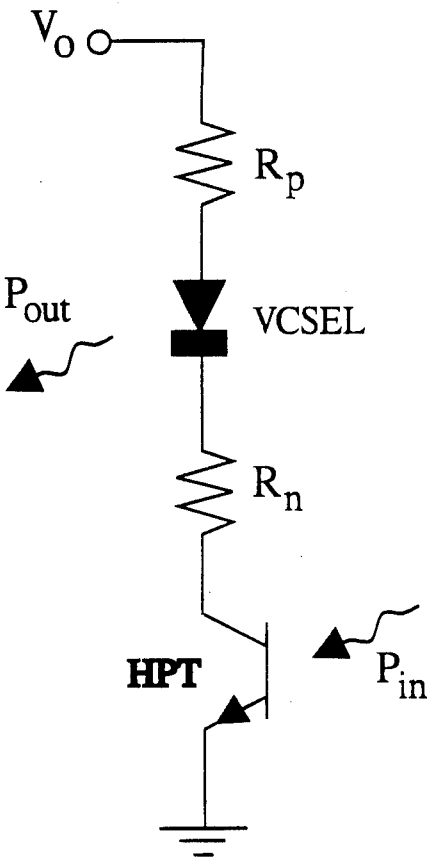


Figure 13: Circuit model of CELL.

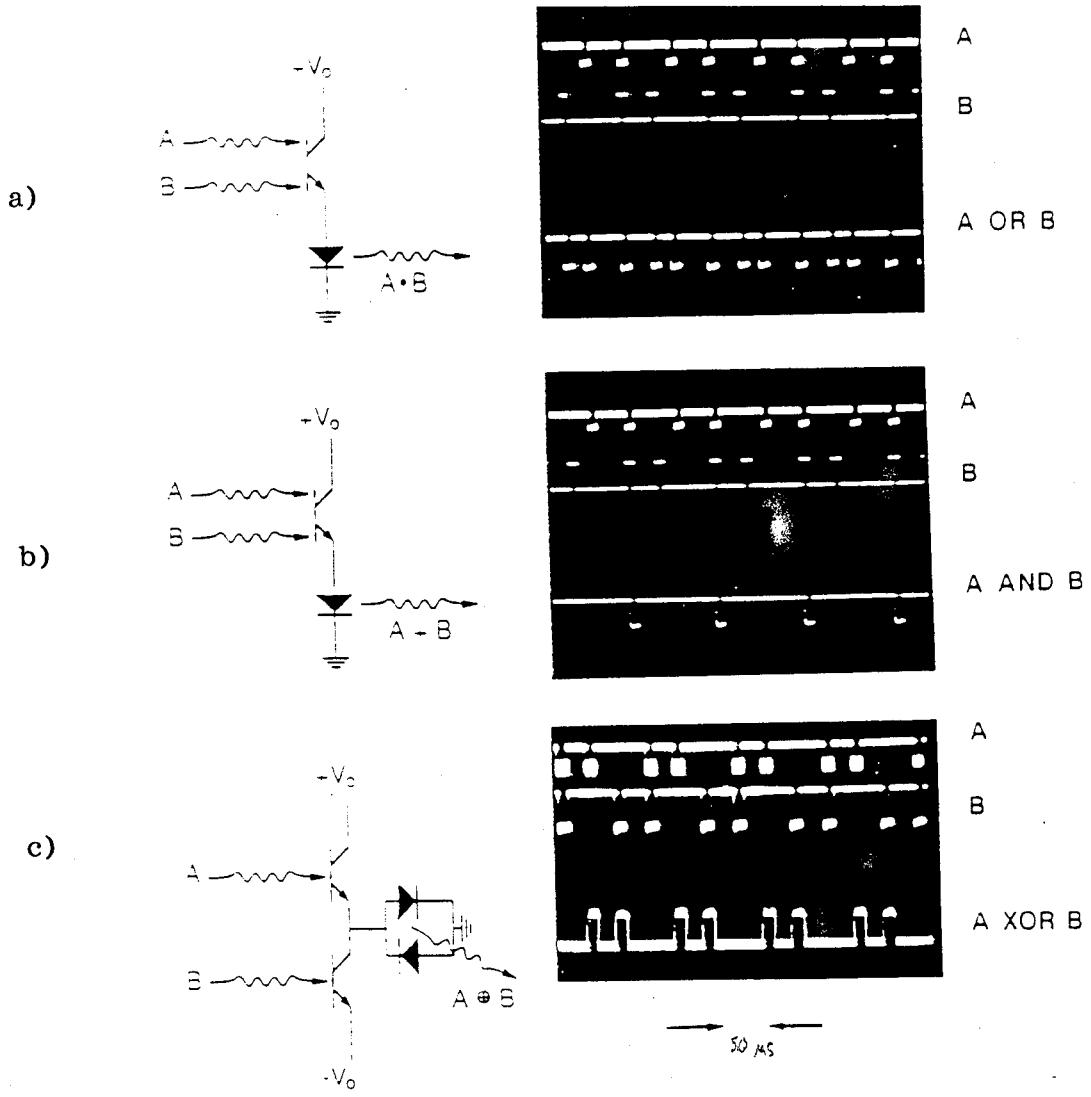


Figure 14: Optical input/output pulse sequences and equivalent circuit configuration for optical OR- and AND-gates using a CELL and an XOR-gate using a simple combination of VCSELs and HPTs.

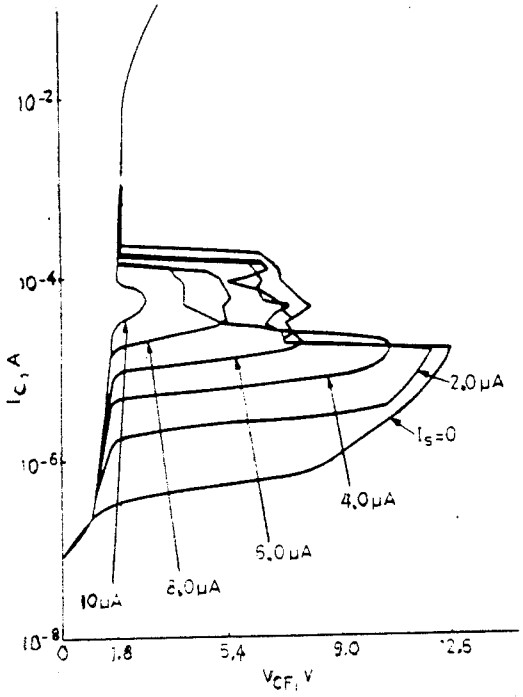
IV. DOES Smart Pixels

As discussed previously, the F-SEED smart pixel incorporates SEEDs to manipulate optical signals and FETs for logic functions. Such hybrids have significant advantages.[14] The double-heterostructure optoelectronic switch (DOES) is another hybrid smart pixel.

The DOES device[15-17] is similar in operation to a thyristor except that it can emit and detect light. As an emitter, it can be fabricated as either an LED or laser. Figure 15a shows the three terminal schematic representation of the ppn (n-channel) device and the corresponding characteristic curves. In operation, the collector C has negative bias with respect to the emitter E. The off-state of the DOES corresponds to the lower branches of the curves that are designated as region 1. Applying negative bias to the inversion channel gate G switches the device from the low to high current state (region 3). These two states are connected by region 2 of the curves which have negative differential resistance. The fact that the current increases with decreasing voltage in region 2 explains why the device is driven towards the on-state once the switching signal is applied. Physically, the switching occurs as a result of adding electrons to the inversion region that forms the active region of the device. The device can be switched to the low current state by removing electrons from the active region. A significant portion of the on-state current pumps the GaAs active layer to produce either the spontaneous or stimulated emission for the LED or laser, respectively.

A cross-sectional physical view of the original nnp DOES[16] appears in Figure 15b. Note that the electrical biasing scheme is the opposite of that discussed for the ppn device

a)



b)

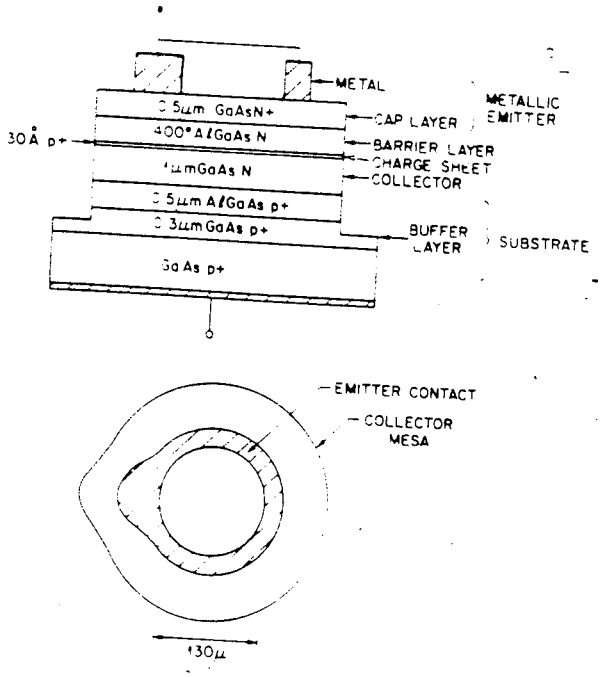


Figure 15: a) 3-terminal switching characteristics of an n-channel DOES. b) Physical structure of the DOES.

above. The structure is grown on p^+ GaAs substrate. The subcollector and collector consist of p^+ AlGaAs and n GaAs, respectively. A thin, highly p^+ doped charge sheet is grown into the collector to produce the desired band bending affect at the interface between the collector and an n-type AlGaAs barrier layer.

The DOES can be used in a variety of circuits as a smart pixel. Figure 16 shows an electrically addressable inverter. There are two outputs in the circuit. One is an optical signal from the DOES. The other is at the node between the load FET 1 and the DOES; in this case, the signal is a voltage. The smart pixel is electrically addressed to switch it between the emitting (ON) and non-emitting (OFF) states, respectively. For the ppn device shown, electrons or holes must be injected into the gate to switch the DOES to the ON or OFF states, respectively. FET 2 switches the DOES to the ON state and BICFET 1 switches it OFF.

In addition to the binary switch, the DOES can function as an optical memory element. As a result of operation similar to a thyristor, the DOES holds its present state until a signal sets or resets it.

V. Diode Laser Logic (DLL)

As previously discussed, the photonic switch is the first step toward all-optical signal processing. Diode Laser Logic (DLL)[18] devices presently under development consist of monolithically integrated multiquantum well semiconductor lasers with intra-cavity modulators electrically connected to photodetectors. DLL presents a full family of logic gates with high fanout and on/off contrast ratio including adjustable width for the

input-output hysteresis. Because of the features of the logic family, optical binary adders and cross bars can be implemented with one gate. In addition, the differential input used by the SEED devices can also be implented with DLL.

Figure 17 shows an OR gate as an example. The laser cavity has a Total Internal Reflection (TIR) mirror at one end to improve the efficiency; in other designs, this TIR mirror is replaced with a flat mirror for access to the laser output. The modulator between the gain section and the flat 34% reflective mirror on the right hand side controls the lasing threshold current of the cavity; the threshold current depends exponentially on the reverse bias voltage. The integrated current source (a carbon resistor or FET) reverse biases the modulator and quenches the laser. Light incident on either photodetector produces photocurrent sufficient to satisfy the current source, forward bias the modulator and activate the laser. The current source is not required for most of the other logic functions.

Figure 18 is a typical linear and logarithmic plot of the emission spectra from an OR gate with external silicon photodetectors. The logic 0 and logic 1 states are shown. Typically, the lasers are 4 x 100 μm in size and the modulators are 4 x 4 μm. A current source of 1 mA is limited to reverse bias voltages of about -4 volts.

The DLL family is most suitable for digital optical processing and communication applications, including ATM packet switching, all optical adders, and optical cross bars. In addition, they are a good choice for the optical transmission of data between electronic chips and circuit boards.

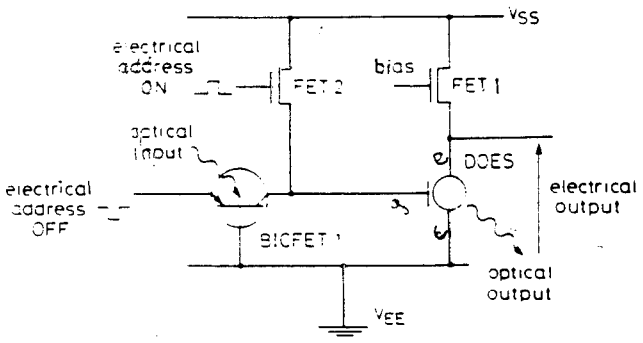


Figure 16: DOES circuit schematic of an electrically addressable inverter.

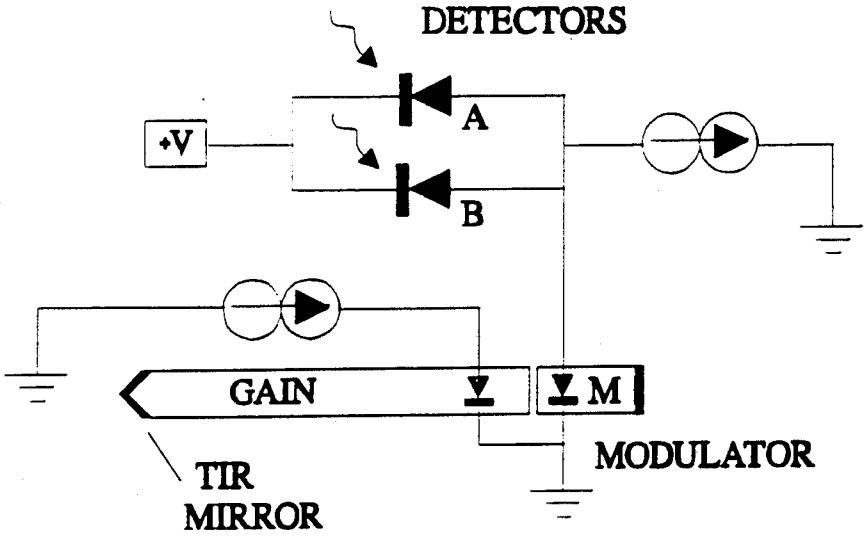


Figure 17: An optical OR gate using Diode-Laser Logic.

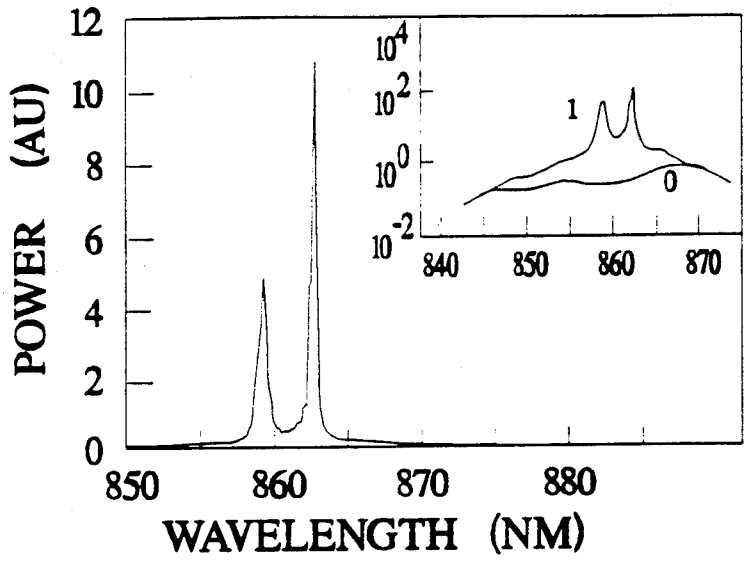


Figure 18: Emission spectra from the DLL OR-gate.

V. Quenched Laser Optical Gates

In addition to the hybrid, there is also the all-optical smart pixel. One such smart pixel consists of a laser that is optically quenched by another laser[19-22] or laser-quenched lasers (LQLs). An LQL gate that performs the Boolean NOR function consists of two inverters as shown in Figure 19. The figure shows a top view of the main laser and the two quench lasers.[20] Each quench laser has two halves that are separated across the main laser but the two halves are electrically connected in parallel. Thus a portion of the two quench laser cavities overlaps the main laser cavity. The portion of the main laser that also forms part of the cavity for the quench laser is the common cavity region. In normal operation, the main cavity is biased just above lasing threshold and the quench lasers are off. The lasing centers in the regions of overlap interact with photons with propagation vectors k_m parallel to the cavity of the main laser. If either quench cavity lases, photons with propagation vectors k_q parallel to the quench laser enter the region of cavity overlap. Both the k_m and k_q photons compete for the same lasing centers in the overlap region. For sufficiently large intensity in the quench lasers, the lasing centers in the overlap region produce stimulated emission parallel to the quench lasers instead of along the main laser cavity. As a result, the gain of the main laser is reduced and the main laser switches off.

The LQL gates are potentially the fastest available laser-based smart pixels. However, for many of the laser-based smart pixels, a circuit amplitude modulates the laser which requires the carrier population in the laser to change. There are several effects that determine the highest possible speed for the modulation, including carrier relaxation time

and cavity lifetime. For LQLs, the carrier population does not have to change, implying that the overall speed of the device must be larger than that for amplitude modulated lasers. On the negative side however, the LQL gates require relatively large amounts of electrical power for the lasers. At present, lasers require on the order of 1 mA at 2 volts (2 mW) to bring them above lasing threshold.

The first patent on the LQLs, by W. F. Kosonocky[23] in 1969, describes the design for overlapped cavities using an amplifier and laser section as shown in Figure 20. Both sections use the same volume of semiconductor material and the same set of electrical contacts. A complete logic family is outlined in the original patent. The next patent, by J. L. Fitz[24] in 1989, improves and changes the original design by separating the amplifier and laser sections into two laser sections similar to the one shown in Figure 19. Each section of the device has its own electrical contact and can be independently biased. A further improvement for optical processing and interconnect purposes, by Parker et. al.[25,26] and Shire et. al.[27], replaces the output laser with a VCSEL where both lasers are fabricated in the same VCSEL heterostructure.

The results[20] from two NOR gates with differing threshold currents for the main laser appear in Figure 21. The graph plots the emitted power from the main laser as a function of the current injected into one of the quench lasers; the power has been normalized to unity. The main laser has a threshold current of 36 mA as determined by a separate set of measurements. The curves are labelled by the values of the current injected into the main laser. Approximately 80% of the optical power from the main laser can be quenched. Note the linear decrease in main laser intensity as the side laser current

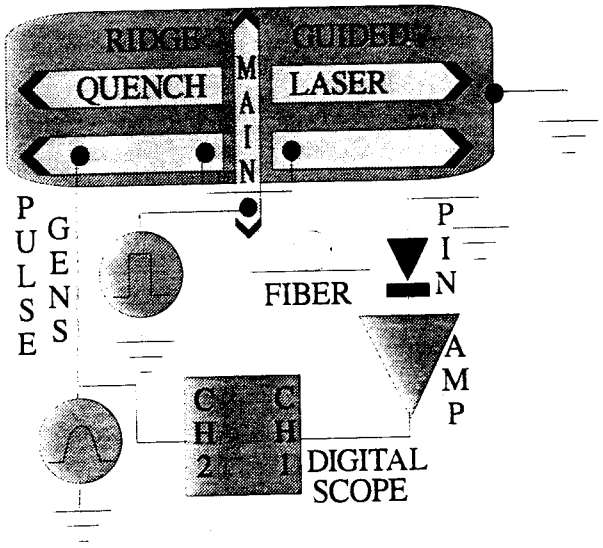


Figure 19: LQL NOR-gate and experimental setup.

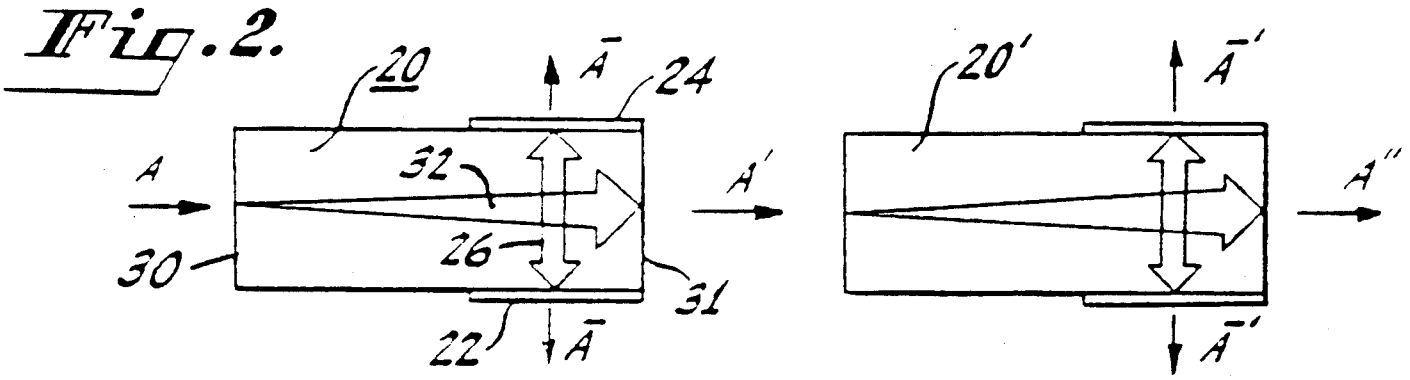


Figure 20: LQL schematic.

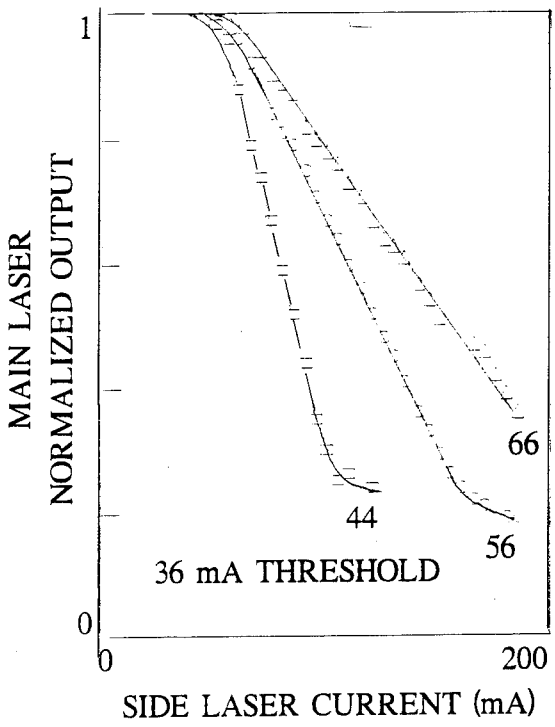


Figure 21: Operation of LQL gates.

increases. Also note that, to maintain a given intensity from the main laser, more side laser current is required for larger main laser currents. Thus, main lasers with larger bias currents are more difficult to quench.

The quench curves in Figure 21 consist of the Spontaneous Emission Region (SER), the Linear Region (LR) and the Saturation Region (SR). The SER corresponds to side laser currents smaller than about 50 mA; this region is due to the lack of stimulated emission in the quench lasers. The irradiance from the main laser can increase to values larger than 1 if the resistance between the main and quench lasers is sufficiently small or if the spontaneous emission from the quench laser aids the pumping of the main cavity. LR refers to that part of the graph where the irradiance from the main laser linearly decreases. For this region, a photon from either the quench or main laser cavity can stimulate the emission of a photon from electron-hole recombination in such a way that the wavevector of this emission is parallel to either the quench or main laser cavity respectively. However, above threshold, the photon density in the quench laser is linearly proportional to the quench laser pump current. Thus the probability of interaction between the photons from the quench laser and electron-hole pairs in the common cavity increases linearly. As a result, the net gain of the main laser linearly decreases to a fixed value. Main lasers operating at higher current densities require larger quench laser currents to achieve the same amount of quench. The SR, the region where the irradiance saturates, occurs for relatively large values of the quench current. For LQL gates with a small volume for the common cavity, the main laser cannot be quenched and the intensity of the stimulated

emission corresponds to the observed saturation level. For volumes of the common cavity sufficiently large to allow for the main laser to be quenched, the observed saturation level is attributable to the intensity of the spontaneous emission from the main laser.

As is evident, smart pixel devices are relatively new and represent an area of intense research. There are numerous types of smart pixels. The devices presented here represent a sampling of those that are currently fairly well established. They can be used in myriads of applications including image and optical-signal processing.

APPENDIX: The Smart Pixel For Dual-Use Applications Including Optical Communications And Signal Processing

This appendix discusses the importance of the optical smart pixel for government and commercial sectors. The text was presented as a paper to Science Advisory Board in June of 1995 (Washington DC).

I. DEFINITION OF THE SMART PIXEL

The smart pixel is an opto-electronic device that functions both as an optical interconnect and as a logic element (analog or digital). It consists of a single device or a small cluster of monolithically integrated devices. As an optical interconnect, it transmits and receives information using light rather than electrical current. The logic function can be as simple as the amplification of an input signal to as complicated as a complete packet switching unit. Some smart pixels receive electrical information and simply convert it to the optical domain or vice versa.

II. WHY ARE SMART PIXELS IMPORTANT?

Smart pixels are photonic devices that form a compact link between the electronic and optical domains. They represent the basic building blocks of future technology since they are built from both electronic and optical components. The definition above embraces a large number of devices. However, when electronic components are part of the pixel, they will generally be Field Effects Transistors (FETs), Heterostructure Bipolar Transistors (HBTs) or Heterostructure PhotoTransistors (HPTs). The optics can include integrated

lenses, photodetectors, lasers, laser amplifiers and Self-Electrooptic Effect Devices (SEEDs).

A. On the Necessity of Opto-Electronics and Photonics

There is presently a debate as to whether the most suitable devices to meet the future needs of the DOD and commercial sectors are all electronic or all optical. Electronic devices represent a trillion dollar industry especially for computer chips. But recently, industry has recognized the inherent advantages of some optical devices especially for Compact Disks, communications and special types of computing using optical images. The analyst naturally questions which technology is better and which one will survive into the 21st century?

This tends to be a complicated question of economics and technology. However, a simple argument proves that, during the next 10 to 20 years, the best suited devices will be opto-electronic (i.e., photonic). The argument proceeds as follows. Electronics is a well-established industry with products that permeate all aspects of our lives. The electronic devices are low cost and highly reliable. In addition, electronic devices can be made significantly smaller than optical ones since, for light to interact with matter, at least several wavelengths (about 1/2 micrometer in GaAs) are required. On the other hand, optics has significantly larger bandwidths (more communications channels) since the electronic devices are limited by the long-range Coulomb interaction between charged particles. This long range interaction is also responsible for the unacceptable cross-talk in

electronic circuits at high modulation frequencies. *Thus optics and electronics compliment one another.* But, *optics and electronics can never be separated* because light must interact with charge for it to be useful. As is evident, photonic devices should continue to become more important.

B. Why Optics?

Communications systems and signal processors are presently limited by the system architecture and by both the performances of the electronic logic elements and the electrical interconnections between those elements. These issues are inter-related since the architecture must be built around the available devices and subsystems. There are four significant problems with present architectures as a result of the inherent limitations of the logic elements and, especially, the interconnects. The *first* is that present electrical devices are slow and they have limited functionality. Here, functionality refers to the number of functions that a single device can perform. This problem can be solved by replacing electronic logic elements with optical ones. This is an area of intense research at present. The *second* is the two dimensional aspect of integrated circuitry where the data signals are confined to a plane. The complexity and density of the interconnections increase faster than that for the devices. Some integrated circuit manufacturers now use multiple levels of metal interconnections between planar logic devices but this approach still has its limitations. The *third* problem is that the interconnects are electrical in nature. The bandwidth is limited by resistance and capacitance effects and the power required to drive the interconnect increases with the driving frequency. These last two problems

can be solved by the use of interconnects that are optical rather than electrical. Most commonly, the future signal processor or communication system is envisioned as a set of stacked wafers that communicate with each other by light. The use of 3-D optical interconnects increases the parallelism of the data link and, hence, also the speed of the system through efficient use of three dimensions. The devices that produce or modulate the light can also be given logic functions. Thus, in effect, one device can serve as a logic element and as an interconnect. Such *smart pixels* are generally viewed as single devices or small clusters of devices. The *fourth*, and perhaps the most significant problem, is that communications between users are generally coordinated by a central computer. Such a controller decreases overall speed due to "bottleneck" issues. However this problem can be eliminated by implementing smart communications fabrics such as a packet switching network where the processing is distributed across the nodes of the network. Such smart nodes can be implemented with optical smart pixels.

C. Example Applications

The fact that there can be so many different types of smart pixels suggests that there are also many different applications. The following list contains example applications.

* Distributed signal processing systems such as neural networks and packet switching networks consist of communication channels (optical fibers for example) that interact at nodes. These nodes intercept information, perform calculations or logic functions and then transmit the results to the next node. The most natural choice of device for the node is the smart pixel.

* A telephone switching network is a prime example. Here, large numbers of telephone lines (fibers) must be interconnected. A smart pixel can be used as the router. As another example for switching networks, suppose that 1000 lines

must be interconnected with another 1000 lines at a local node. Then 1,000,000 interconnections are required. It is possible to replace these interconnections with one dynamically reconfigurable interconnection so long as the reconfiguration speed is fast compared with the data.

* Computers will one day use optical backplanes to transmit signals from circuit board to circuit board rather than using the slower electrical transmission lines used today. Speeds can be increased over 1000 fold by using smart pixels to tap into the optical data flow and converting it to the electronics domain.

* The smart pixel can be used for image processing where, for example, an input image is corrected or enhanced in real time for the viewer or robotics system. These pixels can be integrated as a pre-processor to perform similarly to the retinas in many animals. Incidentally, such a smart pixel based pre-processor would significantly enhance the performance of present computer software for target and image recognition systems.

* Fly-by-light for advanced jet fighters and commercial airlines will use variations of smart pixels for the interfaces between the computers and the actuators at the airfoils. Similarly, photonic fabrics in the airfoils (smart skins) can use local processing to reduce the data flow before passing it on to the main computer set.

As is apparent, the applications are extremely varied.

III. PRESENT DEVELOPMENT STATUS

Smart pixels as opto-electronic devices require further development. There are two considerations for ascertaining the present status. The first consideration is more of an architectural issue in the sense that various materials and techniques for fabrication are available. The second consideration focuses on the devices that are actually available at present.

A. Architecture

At present, VLSI circuitry is implemented in silicon because of its well-established processing technology, high yield and low cost. The technology for processing direct-bandgap materials, such as GaAs, is still in its infancy compared with that for silicon. However, the direct-bandgap materials have several important advantages over silicon: (1) the electronic components integrated in GaAs operate at significantly higher speeds and (2) those components can also emit and detect light with high efficiency. For the near future, this developing technology can support small to medium scale integration with the advantages of high operating speed and the efficient emission, detection and amplification of optical energy. It should be mentioned, that GaAs based electronic logic has been hampered by the lack of "native oxides" for FET gate insulation. Recent progress with GaN and GaS for use as emitters and gate insulators will probably lead to very high speed VLSI opto-electronic circuits. The ultimate benefits derived from the use of direct band-gap technology surpasses those derived from providing light emitting capability for the indirect band-gap materials such as silicon.

Epitaxial liftoff is a very near term solution for producing smart pixels and opto-electronic circuits. For this method, light emitters are fabricated on wafers made from direct-bandgap materials. The devices are chemically separated from the wafer and then mechanically fastened to integrated circuits composed of silicon electronics. There is something to be said for the fact that it works but it will probably prove to be more

expensive to fabricate these circuits than to monolithically integrate them on direct bandgap materials.

Attempts to produce light emitting silicon might one day provide a silicon device that emits light. Such a device is highly desirable since it would provide optical capability for massive silicon industry. Porous silicon as a light emitter is produced by acid etching silicon. At present, the emission efficiency is too low to be practical and only optically pumped devices are available. The situation is unlikely to improve during the next 5 to 10 years and considerable research is required. Silicon-germanium quantum wells are also under consideration as light emitters. Of course there is still the question of emission efficiency. As a result of the quantum wells, the cost of growing the material is increased to that of the direct bandgap materials. In addition, both the cost and complexity of fabricating the devices also increases.

Monolithic integration of opto-electronic devices on direct bandgap materials is the preferable future technology. Presently, there are several companies using or selling electronic and opto-electronic GaAs circuits. Motorola fabricates GaAs microwave circuits for use in portable cellular "flip-phones." Recently, Motorola has also begun marketing Vertical Cavity Surface Emitting Lasers (VCSELs) with optical fiber for use as optical interconnects. Another company, MiniCircuits Inc., has started selling GaAs based switches and amplifiers for about a dollar a piece. It is ideal to use GaAs for these circuits

since RF amplification requires relatively few components but those few components must be fast.

B. Some Specific Devices

Self Electrooptic Effect Devices (SEEDs) represent one of the first smart pixels. In operation, a change in the voltage applied to the device causes a change in the absorption, reflectivity and photocurrent. These smart pixels are arranged in two dimensional arrays. The optical signals are received and transmitted perpendicular to the surface. Although these are direct bandgap devices, they are not designed to generate light on their own; they modulate and reflect back the incident light. The SEEDs can be integrated with FETs to obtain complex logic functions. Recently, AT&T has integrated SEED devices with silicon electronics by the epitaxial liftoff procedures. However, the SEED devices and SEED based systems are very temperature sensitive and require bulk optics (not integrated optics) for their operation.

The monolithic integration of FETs and lasers potentially has the highest near term payoff of all the smart pixels. The lasers can be used as emitters or detectors for optical signals while the FETs provide for the logic. These devices are presently under development at various laboratories including Cornell University and the Photonics Center at Rome Laboratory. These FETs and Lasers are expected to have considerable impact on neural network and packet switching technologies. Companies such as Photonics Research Incorporated (Boulder CO) and Intelligent Automation (MA) are developing the SurfaCe

Emitting Laser Logic (CELL) and the Inversion Channel Technologies, respectively. These smart pixels consist of VCSELs, HPTs , and thyristors that are epitaxially grown on GaAs. The devices are ideal as optical logic gates or amplifiers in 3-D computer architectures.

Vertical Lasers with Optical Gain Control (V-LOGiC) consist of VCSELs and In-Plane Lasers (IPL) with cross-coupled cavities. Laser emission from the IPL *optically* quenches the VCSEL. The patents on the devices describe applications such as optical ATM switches and spontaneous emission filters for laser amplifiers (Cornell University and Rome Laboratory, alphabetical order). Gain quenching has the highest modulation bandwidth out of any of the methods for modulating semiconductor lasers. Configurable Optical Gates (COGs) are another laser-based smart pixel (patent with Cornell University and Rome Laboratory, alphabetical order). Integrated detectors drive a modulator section within the cavity of the laser. The COGs form a complete Diode Laser Logic (DLL) family with all of the basic Boolean logical functions. In addition, the COGs greatly simplify the design of optical adders and optical crossbars. Variations of the COGs should find considerable application in switching networks and fly-by-light systems.

Smart pixels have applications in the area of optical memory and mass storage. Besides the use for reading or writing optical disks, the smart pixels can be configured as memory elements. Low Temperature GaAs and amorphous silicon are presently being investigated for weighting functions for neural networks. In addition, the advent of GaN

lasers (Cornell University and Rome Laboratory, among others) promises to increase the storage capability of optical disks considerably.

There is research by groups on lithium niobate devices. But the devices are slow and require bulk optics.

IV. DEPARTMENT OF DEFENSE APPLICATIONS

Surveillance requires high speed signal processors for radar, target detection, target identification, and jamming. Parallel 3-D architectures potentially offer the highest computational throughput for these purposes. Command and Control requires structures with multiple, dispersed nodes and distributed function (distributed processing systems). These distributed systems increase the speed, flexibility and survivability of the strategic systems. Communications need ATM and PACKET switches for tactical battlefield communications scenarios. Intelligence requires neural networks as an intelligent link between sensors and personnel for data classification purposes. The potentially large number of sensors place stringent requirements on the processing, such as correlation and fusion, and routing of data. As another example, it has been predicted that the time required to break codes can be greatly reduced by using opto-electronic computers consisting of quantum dots. Signal processing thrusts develops scalar, vector and special purpose signal processors. These thrusts explore the fusion of data from multiple surveillance radar units and IR cameras, advanced architectures, wafer scale vector processors, and integrated RISC processors. Avionics requires modules for fly-by-light

and smart skins. All of these requirements can be addressed by distributed optical signal processing systems that use photonic smart pixels as the basic building blocks.

V. RELATIONSHIP TO COMMERCIAL DEVELOPMENTS AND APPLICATIONS

Present commercial developments are in optical interconnects, light emitters, GaAs electronics, personal communications services. The applications discussed in sections II and IV are just beyond the cutting edge of technology and require further research and development. The work should continue to invent new components as alternatives to existing ones. Often there is the opinion that if existing components are available and serve the purpose then there is no need to invent new, untested technology. However, new ideas translate to new and improved systems, economic growth, and improved defensive capabilities in addition to the transfer of dual use technology, patents, publications and funding. The work should explicitly investigate new technology and employ the already developed technology when appropriate.

It is possible for government and academic laboratories to develop new technology and then transition it to the commercial sector for further development. Usually this requires well-developed concepts since the commercial sector tends to prefer near term payoffs. The laboratories are useful for this initial development since there is not the same degree or type of pressure for a product that can be sold. However, personnel in these laboratories need to be more aware of the needs and trends in other areas. Continued

emphasis and practice of the basic premises of technology transfer and programs that support dual use technology should improve the situation.

VI. IMPACT ON AFFORDABILITY

Many of the devices are not available at this time. Once fully developed, commercialization will obviously reduce the unit cost, increase reliability and increase performance.

VII. RECOMMENDED DEVELOPMENT

Present trends in communications should continue. Historically, communication has progressed through printing, AM and FM radio, television, cable TV, the internet and satellites. This growth will continue and the next 20 years will be critical. Development of distributed processing systems such as the packet switching network will be necessary for handling the massive routing problems associated with that growth.

Improvements in communications naturally implies increasing demands for mass storage systems and ultra high speed computers. These increasing demands are a result of many factors including economic growth, computerization of banking and business, growth in the film and music industry, increases in knowledge such as that found in professional journal publications and expansions in aviation routing. As a result, optical memory in the form of integrated memory devices and mass storage systems will become more important. In addition, signal processors must become faster to sort through the data and also to meet the demands of future signal processing.

Research will begin on new types of computers. The opto-electronic signal processor will certainly be an area of intense interest in all sectors. Special attention must be given to the growth and fabrication of direct bandgap materials. As previously mentioned, a processor based on quantum dots might prove to make present security coding obsolete. Molecular computers that use molecules as the computing element might become more intensely researched especially if a DNA type of growth mechanism can be used to fabricate these devices. Neural networks will be essential for many diverse applications including pattern and target recognition, oversight of manufacturing processes and the automation of many medical procedures or artificial limbs.

REFERENCES

1. J. W. Goodman, F. J. Leonberger, S. L. Kung, R. A. Athale, "Optical Interconnects for VLSI Systems," Proc. IEEE 72, 850 (1984).
2. A. L. Lentine, D. A. B. Miller, "Evolution of the SEED Technology: Bistable Logic Gates to Optoelectronic Smart Pixels," IEEE J. of Quantum Electronics, 29, 655 (1993).
3. M. E. Prise, N. C. Croaft, R. E. Lamarche, M. M. Downs, S. J. Walker, L. A. D'Asaro, L. M. F. Chirovsky "Module for Optical Logic Circuits Using Symmetric Self Electro-Optic Effect Devices," Appl. Opt. 29, 2164 (1990).
4. G. D. Boyd, D. A. B. Miller, D. S. Chemla, S. L. McCall, A. C. Gossard, J. H. English, "Multiple Quantum Well Reflection Modulator," Appl. Phys. Lett. 17, 1119 (1987).
5. N. Peyghambarian, S. W. Koch, A. Mysyrowicz, Introduction to Semiconductor Optics, Prentice Hall (Englewood Cliffs, NJ) 1993, page 266.
6. D. A. B. Miller, D. S. Chemla, S. Schmitt-Rink, "Relation Between Electroabsorption in Bulk Semiconductors and in Quantum Wells: The Quantum-Confined Franz Keldysh Effect," Phys. Rev. B33, 6976 (1986).
7. D. A. B. Miller, L. M. F. Chirovsky, T. Lentine, T. Woodward, R. McCormick, S. Hinton "FET-SEED Design Workshop," June 21, 1993. AT&T Bell Laboratories, 600 Mountain Ave., P. O. Box 636, Murray Hill, NJ 07974-0636.
8. E. A. De Souza, L. Carraresi, G. D. Boyd, D. A. B. Miller "Analog differential Self-Linearized Quantum-Well Self-Electro-Optic-Effect Modulator," Opt. Lett. 18, 974 (1993) and references therein.
9. L. A. D'Asaro, L. M. F. Chirovsky, E. J. Laskowski, S. S. Pei, T. K. Woodward, A. L. Lentine, R. E. Leibenguth, M. W. Focht, J. M. Freund, G. G. Guth, L. E. Smith, "Batch Fabrication and Operation of GaAs-$Al_xGa_{1-x}As$ Field-Effect Transistor-Self-Electrooptic Effect Device (FET-SEED) Smart Pixel Arrays," IEEE J. Quantum Electr. 29, 670 (1993).
10. H. Hida, A. Okamoto, H. Toyoshima, K. Ohata, "An Investigation of i-AlGaAs/n-GaAs Doped-Channel MIS-like FET's (DMTs) -- Properties and Performance potentialities," IEEE Trans. Electr. Dev. ED-14, 1448 (1987).
11. H. C. Casey Jr., D. D. Sell, K. W. Wecht, "Concentration Dependence of the Absorption Coefficient for n- and p-type GaAs between 1.3 and 1.6 eV," J. Appl. Phys. 46, 250 (1975).
12. T. K. Woodward, A. L. Lentine, L. M. F. Chirovsky, S. S. Pei, J. M. Freund, L. A. D'Asaro, M. F. Focht, E. J. Laskowski, G. D. Guth, L. E. Smith, "Operating characteristics of GaAs/AlGaAs FET-SEED Smart Pixels" IEEE International Electron Devices Meeting Technical Digest, Dec 13-16, 1992, Page 92-655.
13. Photonics Research Incorporated, 325 Interlocken Pkwy., Building A, Broomfield, CO, 80021.
14. J. Cheng, P. Zhou, S. Z. Sun, S. Hersee, D. R. Myers, J. Zolper, G. A. Vawter, "Surface-Emitting Laser-Based Smart Pixels for Two-Dimensional Optical Logic and Reconfigurable Optical Interconnections," IEEE J. Quantum Electr. 29, 741 (1993).
15. P. A. Kiely, G. W. Taylor, D. P. Docter, P. R. Claisse, T. Vang, P. A. Evaldsson, S. K. Sargood, S. Daryanani, P. Cooke, K. F. Brown-Goebeler, "Demonstration of a smart pixel using DOES device technology," IEE Proceedings-J, Vol. 139, No. 3, 208 (1992).
16. G. W. Taylor, J. G. Simmons, A. Y. Cho, R. S. Mand, "A new double heterostructure optoelectronic switching device using molecular beam epitaxy," J. Appl. Phys. 59, 596 (1986).
17. G. W. Taylor, J. G. Simmons, "The bipolar inversion channel field effect transistor (BICFET) -- a new field effect solid state device: theory and structure," IEEE Trans. ED-32, No. 11, 2345 (1985).

18. M. A. Parker, P. D. Swanson, J. S. Kimmet, S. I. Libby, "Diode Laser Logic for Use as Smart Pixels for Optical Signal Processing," SPIE OELASE Optoelectronic Signal Processing for Phased-Array Antennas IV Conference Proceedings, Vol. 2155, P. 124 (1994).
19. G. J. Lasher, "Analysis of a Proposed Bistable Injection Laser," Sol. State Electr. 7, 707 (1964).
20. M. A. Parker, S. I. Libby, P. D. Swanson, "An Optical NOR Gate Based on GaAs- AlGaAs Heterostructure Lasers, "IEEE C3I Conference, Utica, NY (June 1992).
21. W. J. Grande and C. L. Tang, "Semiconductor Laser Logic Gate Suitable for Monolithic Integration," Appl. Phys. Lett. 51, 1780 (1987).
22. C. L. Tang, A. Schremer, T. Fujita, "Bistability in Two-Mode Semiconductor Lasers Via Gain-Saturation," Appl. Phys. Lett. 51, 1392 (1987).
23. W. F. Kosonocky, U. S. Patent 3,431,437 (Mar. 4, 1969); filed May 25, 1964 .
24. J. L. Fitz, U. S. Patent 4,825,442 (Apr. 25, 1989); filed Apr. 19, 1988.
25. M. A. Parker, D. B. Shire, C. L. Tang, P. D. Swanson, R. J. Michalak, J. S. Kimmet, Vertical-cavity-surface-emitting Lasers with Optical GaIn Control (V-LOGIC), Patent Application in Mar. 1995.
26. M. A. Parker, P. D. Swanson, S. I. Libby, J. S. Kimmet, C. L. Tang, D. B. Shire, "Spontaneous Emission Filtered Laser Amplifiers," patent filed Dec. 1994.
27. D. B. Shire, M. A. Parker, C. L. Tang, P. D. Swanson, J. S. Kimmet, "Gain Control of Vertical Cavity Surface Emitting Lasers with Intra-cavity Coupled In-Plane Lasers," Accepted for publication in Appl. Phys. Lett. for Spring 1995.

☆U.S. GOVERNMENT PRINTING OFFICE: 1995-610-126-20045

MISSION

OF

ROME LABORATORY

Mission. The mission of Rome Laboratory is to advance the science and technologies of command, control, communications and intelligence and to transition them into systems to meet customer needs. To achieve this, Rome Lab:

a. Conducts vigorous research, development and test programs in all applicable technologies;

b. Transitions technology to current and future systems to improve operational capability, readiness, and supportability;

c. Provides a full range of technical support to Air Force Materiel Command product centers and other Air Force organizations;

d. Promotes transfer of technology to the private sector;

e. Maintains leading edge technological expertise in the areas of surveillance, communications, command and control, intelligence, reliability science, electro-magnetic technology, photonics, signal processing, and computational science.

The thrust areas of technical competence include: Surveillance, Communications, Command and Control, Intelligence, Signal Processing, Computer Science and Technology, Electromagnetic Technology, Photonics and Reliability Sciences.